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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N 09/630,844	Applicant(s) CHASMAWALA ET AL.	
	Examin r Clifford H Knoll	Art Unit 2112	

-- The MAILING DATE f this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 29 December 2003.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-42 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-42 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Rejection of claims 5 and 27 under 35 U.S.C. 112, second paragraph, has been withdrawn.

Claim Rejections - 35 USC § 102

Claim 1-30 stand rejected under 35 U.S.C. 102(e) as being anticipated by von der Wense (US 6598107).

Regarding claim 1, von der Wense discloses a memory storing program code and a processor connected to memory operable to execute the program code (e.g., col. 1, lines 15-18, "microcontrollers ... controlling"), bus interface logic coupled to the embedded processor, wherein the bus interface logic is operable to couple to an interconnecting bus, wherein the bus interface logic is adapted to interface with a device through the interconnecting bus (e.g., col. 1, lines 21-27, "actuators, sensors, etc. are combined with a corresponding microcontroller of the unit, and control wires between each unit ... are reduced"), wherein the embedded processor is operable to execute the program code to perform a CAN event in response to said bus interface logic receiving a trigger signal from the device (e.g., col. 1, lines 28-30, "for communicating data between the units a multiplexed serial bus is provided"), wherein in response to receiving the trigger signal, the embedded processor is operable to perform the CAN

event substantially synchronously with an event performed by the peripheral device (e.g., col. 5, lines 42-44).

Regarding claim 3, von der Wense also discloses the CAN event comprising transmitting a CAN frame on the CAN bus (col.1, lines 32-33).

Regarding claim 5, von der Wense discloses the logic operable to receive the trigger signal on a first line of a plurality of lines on the bus (col.5, lines 7-9), and an embedded processor operable to receive configuration information from the host computer selecting the first line among a plurality of lines (col.5, lines 9-11).

Regarding claim 7, von der Wense discloses a memory configured to store program code (col.5, lines 8-31) and embedded processor configured to execute the program code (col.5, lines 36-37), bus interface logic coupled to the embedded processor adapted to interface with a device (col.4, lines 55-64), CAN interface logic (col.5, lines 42-50), where the bus interface logic is configured to asset a trigger signal on the interconnecting bus to the device in response to the embedded processor performing a CAN event (col.5, lines 9-11)

Regarding claim 8, von der Wense also discloses the CAN event substantially synchronous with a peripheral device event (col.5, lines 42-44).

Regarding claim 9, von der Wense also discloses the CAN event comprising transmitting a CAN frame (col.1, lines 32-33).

Regarding claim 10, von der Wense also discloses the CAN event comprising receiving a CAN frame (col.5, lines 5-9).

Regarding claim 11, von der Wense also discloses receiving an indication of a function call invoked by a user application program running on the host computer (col.1, lines 54-63).

Regarding claim 12, von der Wense discloses the logic operable to receive the trigger signal on a first line of a plurality of lines on the bus (col.5, lines 7-9), and an embedded processor operable to receive configuration information from the host computer selecting the first line among a plurality of lines (col.5, lines 9-11).

Regarding claim 14, von der Wense discloses receiving a trigger signal on the interconnecting bus from the device (col.5, lines 42-50), perform a CAN event in response receiving a trigger signal on the interconnecting bus from the device (col.5, lines 42-50), and the CAN event substantially synchronous with a peripheral device event (col.5, lines 42-44).

Regarding claim 15, von der Wense also discloses the CAN event comprising transmitting a CAN frame (col.1, lines 32-33).

Regarding claim 19, CAN interface to perform a CAN event, and CAN interface transmitting a trigger signal to the peripheral device through the interconnecting bus in response to the CAN interface performing the CAN event (col.5, lines 9-11), wherein the trigger signal is operable to direct the device to perform an event (col.5, line 11).

Regarding claim 20, von der Wense also discloses the CAN event comprising transmitting a CAN frame (col.1, lines 32-33).

Regarding claim 21, von der Wense also discloses the CAN event comprising receiving a CAN frame (col.5, lines 5-9).

Regarding claim 22, von der Wense also discloses receiving an indication of a function call invoked by a user application program running on the host computer (col.1, lines 54-63).

Regarding claim 24, von der Wense discloses a peripheral device coupled to the host computer system (col.5, lines 8-31), a CAN bus (col.1, lines 32-33), one or more CAN devices (col.1, lines 28-29), an interconnecting bus (col.1, lines 15-21), where the CAN interface device and peripheral device are operable to communicate with each other using the interconnecting bus to synchronize measurement and/or control operations on the physical system (col.5, lines 7-11).

Regarding claim 25, von der Wense also discloses bus interface logic (col.5, lines 10-11) and CAN interface logic (col.3, lines 10-18).

Regarding claim 26, von der Wense also discloses the device operable to provide a signal over the interconnecting bus to the CAN interface device in response to a peripheral event occurring in the peripheral device (col.3, lines 3-6), the CAN interface operable to receive the signal from the interconnecting bus and to perform a CAN event in response to receiving the signal (col.5, lines 7-9).

Regarding claim 27, von der Wense also discloses one or more of initiation of a signal transmission from the peripheral device to the physical system; acquisition of a signal from the physical system (col.5, lines 7-9).

Regarding claim 28, von der Wense also discloses transmitting a CAN frame or generating a signal timestamp (col.3, lines 19-23).

Regarding claim 29, CAN interface to perform a CAN event, and CAN interface transmitting a trigger signal to the peripheral device through the interconnecting bus in response to the CAN interface performing the CAN event (col.5, lines 9-11), wherein the trigger signal is operable to direct the device to perform an event (col.5, line 11).

Claim Rejections - 35 USC § 103

Claims 1-42 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Rao (US 2003/0028701) in view of von der Wense, further in view of Pinto ("Networked, intelligent I/O, the truly distributed control revolution", ISA Proceedings, December 1999).

Regarding claim 1, Rao discloses a memory configured to store program code and embedded processor configured to execute the program code (e.g., paragraph [0019], figure item 100), bus interface logic coupled to the embedded processor adapted to interface with a device (e.g., paragraph [0019], figure item 142), local I/O bus interface logic and the processor operable to execute the program code to perform an event in response to the bus interface logic receiving a trigger signal on the interconnecting bus from the device (e.g., paragraph [0019], figure item 166).

Regarding claims 14 and 19, Rao discloses the local I/O interface receiving a trigger through an interconnecting bus and the local I/O interface receiving the trigger signal and performing an I/O event substantially synchronously (e.g., figure item 138).

Regarding claim 24, Rao discloses a host computer system (e.g., figure items 100, 108), a peripheral device coupled to the host computer system (e.g., figure item 142), a local I/O bus and one or more coupled devices (e.g., figure item 118) wherein the interface device is directly coupled to the peripheral device operable to synchronize measurement and/or control operations (e.g., figure items 146, 138).

Regarding claim 31, Rao discloses the interface acquiring data frames from the bus (e.g., figure item 146, 138), generating timestamps (e.g., figure item 119), transmitting a trigger signal on the interconnecting bus in response to a peripheral event (e.g., figure item 138), receiving the trigger signal and generating a trigger timestamp (e.g., figure item 166), and determining one or more of the data frames which correlate in time with the peripheral event (e.g., paragraph [0036], Figure 6).

Regarding claim 37, Rao discloses a peripheral device transferring data values (e.g., paragraph [0017], figure items 112, 144), the peripheral device generating peripheral timestamps indicating times of transference (e.g., paragraph [0037], Figure 6), an interface performing a frame transfer (e.g., paragraph [0017], figure items 118, 146), a trigger signal a trigger timestamp generated and determining from the peripheral timestamps the one or more of the data values (e.g., paragraph [0037]).

Further regarding claims 1, 14, 19, 24, 31, 37, Rao also discloses a second bus being a local I/O bus and discloses various embodiments thereof (e.g., [0016]). Rao does not expressly mention the CAN bus protocol as a particular embodiment; however this feature is disclosed by von der Wense (e.g., col.1, lines 23-33). Von der Wense discloses a CAN bus as a particular embodiment of a local I/O bus (e.g., col.1, lines 23-

24). It would be obvious to use the CAN bus von der Wense as the local I/O bus of Rao, because a CAN bus is well known as a particular embodiment of a local I/O bus which Rao discloses. This is exemplified by Pinto. Pinto discloses the CAN bus as particular protocol for standard local I/O bus architectures. Therefore it would be obvious to a person of ordinary skill in the art to combine Rao with von der Wense, further as exemplified by Pinto at the time the invention was made.

Regarding claims 4 and 16, Rao also discloses generating a timestamp and storing the timestamp (e.g., paragraph [0037], Figure 6).

Regarding claim 18, Rao also discloses transmitting the trigger signal in response to performing a data transfer (e.g., figure items 138, 166).

Regarding claim 27, Rao also discloses one or more of initiation of a signal transmission from the peripheral device to the physical system; acquisition of a signal from the physical system (e.g., figure items 116, 117, 118).

Regarding claim 32, Rao also discloses analyzing the physical system using I/O data frames that correlate in time with the peripheral event (e.g., figure item 166).

Regarding claim 33, Rao also discloses the determining performed by the I/O interface (e.g., figure item 138).

Regarding claim 34, Rao also discloses read the data frames, I/O timestamps and trigger timestamps and the determining is performed by the host computer system (e.g., figure items 112, 166).

Regarding claim 35, Rao also discloses the event comprising one of the device transmitting signals to the physical system; acquiring signals from the physical system; a clock signal transition (e.g., Figure 6).

Regarding claim 38, Rao also discloses acquiring the data from the physical system (e.g., [0017], figure item 108).

Regarding claim 39, Rao also discloses transmitting data to the physical system (e.g., [0017], figure item 108).

Regarding claim 40, von der Wense also discloses receiving a CAN frame (col.5, lines 5-9).

Regarding claim 41, von der Wense also discloses transmitting a CAN frame (col.3, lines 19-23).

Claims 6, 13, 17, 23, 30, 36, 42 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Rao in view of von der Wense and Pinto as applied in claims 1, 14, 19, 24, 31, 37 above, further in view of Barkesseh (US 6208919).

Rao discloses a method for correlating measurements in a system comprising a host computer system with an interconnecting bus (e.g., figure items 142, 138, 112) but does not expressly mention the interconnecting bus comprising the REAL-TIME SYSTEM INTEGRATION (RTSI) bus. However, this feature is disclosed by Barkesseh. Barkesseh discloses the RTSI bus for synchronizing data signals (col.2, lines 54-55). It would be obvious to combine Barkesseh with Rao, because the RTSI bus of Barkesseh is intended for use precisely in a monitoring test environment that comprises a local and

host bus such as the invention of Rao. Therefore it would be obvious to a person of ordinary skill in the art to combine Barkesseh with Rao and von der Wense at the time of the invention.

Response to Arguments

Applicant's arguments filed 29 December 2003 have been fully considered but they are not persuasive.

Applicant argues that "there are two different buses in the system, whereas in the system of von der Wense, only one bus is used" (p. 11); however this is not correct. von der Wense discloses devices and their connection to the embedded processor; these devices may consist of "actuators, sensors, etc. [which] are combined with a corresponding microcontroller" and that "local data ... are processed in the local microcontroller of the unit" (col. 1, lines 21-25). This combination and the subsequent processing establishes an interconnecting bus, and distinguishes it from a bus established by the subsequent need of "communicating data between the units" (col. 1, lines 28). This is in fact quite the conventional arrangement and use of a CAN bus: von der Wense discloses that the communication hitherto associated with individual control lines between the aforementioned devices is accomplished by this additional bus system, where the embodiment preferred by von der Wense is the CAN bus, which

"provides the communication backbone in up to date cars" (col. 1, lines 28-33). Therefore von der Wense does in fact disclose the two buses that are claimed.

Applicant further argues that von der Wense does not disclose triggers, and fails to teach "the CAN event and the device event being performed substantially in synchrony" (pp. 11-12); however this is precisely the operation of the CAN bus standard as disclosed in von der Wense. Any distinction the Applicant makes for the claimed "trigger", or "synchrony" apart from operation of the CAN bus of von der Wense must be positively recited in the claims. Examiner has included background material on the CAN bus to further elucidate particular details of its operation. Therefore von der Wense discloses the trigger and substantially synchronous event as claimed and rejection of claim 1 is maintained supra.

Applicant essentially repeats these arguments for claims 7, 14, and 19, except in these cases the CAN event is the "trigger" to the interconnecting bus. However, it is clearly established in von der Wense that devices are "addressed" (e.g., col. 1, line 57) and thus they read as well as write data on the CAN bus. Again, reference to the background material on the CAN bus may serve to elucidate standard CAN protocol.

Regarding claim 19 in particular, Applicant argues that the cited passage from von der Wense "merely states 'according to the new ratio the period of the signal pattern is updated then'" fails to disclose a CAN event (p. 15); however all operations of the CAN bus in von der Wense are "CAN events" because von der Wense chooses this embodiment. The citation from von der Wense from the Background of the Invention may help to clarify this: "when they are addressed on the bus again the units must start

up" (col. 1, lines 56-58). All references to bus operations in von der Wense can be viewed in the context of the CAN bus which von der Wense teaches as his preferred embodiment (col. 1, lines 30-33). In all references made by von der Wense to the bus operations occurring between units, implicit reference to the CAN bus protocol is unmistakable. Therefore von der Wense discloses a CAN event as stated in a previous Office Action, and rejection of claims 7, 14, and 19 is maintained.

Regarding claim 24, Applicant argues that von der Wense fails to disclose "using the interconnecting bus to synchronize measurement and/or control operations on the physical system" (p. 16); however, a physical system is implicitly part of the von der Wense system which teaches the operation of "actuators, sensors, etc."; again, as stated supra regarding claim 1, this is quite the conventional arrangement and use of a CAN bus, where in the case of von der Wense, the physical system is a car (col. 1, line 33).

Therefore rejection of claims made in a previous Office Action under von der Wense is maintained.

Regarding claim 1, Applicant references the manner of synchronization of Rao, referring to Rao in paragraphs 36-37) and argues that Rao fails to teach the system of claim 1, apparently distinguishing the form of synchronization (p. 18). However, the cited reference to Rao maintained in the above rejection is the appropriate citation. Rao discloses that results of event counters may be accessed on the bus being monitored (i.e., "first bus 112"), "in response to instructions stored and executed by the host system" (paragraph [0019]). Examiner argues thereby that an event is performed on

the monitored bus and that this event occurs substantially synchronously. Any distinction from the synchronization of Rao must be positively recited in order to receive consideration.

Applicant further argues regarding claim 1, and subsequently for claims 14 and 19, that the combination is merely hindsight and none of the references "provide or even hint at a motivation to combine" (p. 19); however, the motivation is clear and is reiterated here in somewhat more detail in interests of clarification. First a brief summary of the prior art features relevant to the combination: Rao discloses a monitoring environment for a class of buses (e.g., paragraph [0016]) but does not expressly mention that a CAN bus is of this class. Pinto, writing an expository article on the bus class of Rao notes that the CAN bus exemplifies this class. Von der Wense discloses an operating CAN bus and teaches the CAN bus to be an advantageous bus for communicating between units; this in particular has been established clearly based on citations added supra from the background section of von der Wense. Now, if a bus finds advantage in an application, and a base reference teaches a means to monitor buses in this class; the motivation to combine is straightforward. The monitoring apparatus of Rao taught for a class of buses finds application in a bus seen to convey advantages in the particular environment of von der Wense. Therefore, Examiner deems the combination under 103 to be appropriate and maintains the rejection of claims 1 and 14 supra.

Regarding claims 14 and 19, Applicant further argues that Rao "in no way illustrates a CAN interface performing the CAN event substantially synchronously" (p.

19); however, the CAN bus is disclosed by von der Wense as a particular embodiment of the interface of Rao, while the synchronous event disclosed by Rao has been discussed supra regarding claim 1.

Regarding claim 24, Applicant argues that Rao does not teach "the interface device is directly coupled to the peripheral device operable to synchronize measurement and/or control operations" (p. 19); however, Examiner maintains that measurement and/or control operations are indeed synchronized. Applicant argues that the DMA is not an interface device; this is true, but its citation refers to a control operation. All manner of operations on the local bus of Rao including, for example DMA, are synchronized by the event counters which are also cited as part of the peripheral device (figure item 142). Event counters do not asynchronously increment, this is implicit in the definition of an event counter; rather, as detailed above, they increment substantially synchronously with the event they are intended to monitor. Therefore Examiner maintains disclosure of the synchronous event in Rao.

Regarding claim 31, Applicant argues that "nowhere in the cited passage does Rao teach, suggest or even mention data frames" (p. 19); however Rao does teach data frames in disclosing "bus transactions" (paragraph [0036]). A transaction is the means whereby Rao frames data. It is not clear what distinction Applicant wishes to draw, but whatever limitation to data frames is considered must find positive recitation in the claims. Therefore Examiner maintains data frames have been adequately disclosed, and maintains the rejection of claims 1, 14, 19, 24, and 31 under Rao in combination is maintained supra.

Regarding claim 37, Applicant discounts the peripheral device of Rao because it is "located in the monitoring facility of the integrated circuit data processor; however any distinction from Rao as to its location or designation as peripheral finds no positive recitation in the claims. The monitoring facility of Rao is certainly peripheral to the processor which executes the monitoring function via a common bus; *a forteriori*, the processor "may be implemented on a separate die" (paragraph [0017]). Therefore Rao does in fact disclose a peripheral device and rejection of claim 37 is maintained.

Applicant argues "in a more general sense" that both primary references relate to synchronization in a different meaning (p. 21); however, hopefully the extended discussion supra serves to clarify the synchronization feature in both rejections which Examiner maintains reads on the invention as recited in the claims.

Applicant distinguishes the claimed invention as drawn toward signals used for stimulus response behaviors; however, to the extent that these features are recited, they have been found by the Examiner in a previous Office Action and maintained supra to have been anticipated and/or obvious.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Siemens ("Controller Area Network") has been cited for background purposes to elucidate certain aspects of the CAN bus.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 703-305-8656. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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